מעבדה  לאבטחת חומרה

Security Counters for RISCV processor

Recently we proposed and implemented the notion of Security counter as part of RISCV processor.

The idea is to be able to count the number of events that occur within an interval of time or an interval of code.

In this project, you are requested to extend this idea and to write software that can demonstrate its capabilities.

prerequisites

- Computer Architecture course.
- Knowledge FPGA is plus

Expected results

(1) understanding the current implementation.
(2) Developing the SW package to support it
(3) Extending the idea

The project can be extended to another semester if the student/team decides to develop Software that will take advantage of the new proposed system

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